

In The Claims

1. (Currently Amended) A method for fabricating a device on a substrate, comprising:
forming first and second isolation regions in said substrate, said first isolation region bordering a first side of an active area of the device and said second isolation region bordering a second side of said active area opposite said first side;
forming a gate over said substrate, said gate extending between said first and second sides of said active area;

forming a source/drain extension region in said substrate on each side of said gate, said source/drain extension regions extending between said first and second sides of the active area and including dopants of a first conductivity type;

forming at least one corner diffusion region first and second corner diffusion regions in said substrate, said corner diffusion regions including dopants of a second conductivity type that is opposite to said first conductivity type and overlapping with at least a portion of one of said a first source/drain extension regions region in areas of said substrate adjacent said first and second isolation regions; and

forming source and drain diffusion regions in said substrate adjacent said source/drain extension regions on opposite sides of said gate and extending between said first and second sides of said active area, said source and drain diffusion regions being further away from said gate than said source/drain extension regions and including dopants of said first conductivity type.

2.-3. (Cancelled)

4. (Currently Amended) The method of claim 1 wherein said device occupies an active area of said substrate, and wherein forming corner diffusion regions comprises applying a mask on said substrate that exposes at least a portion of said active area near said gate.

5. (Currently Amended) The method of claim 4 wherein said active area is bordered on some or all sides by isolation regions in said substrate, said exposed portion of said active area being near at least one of said isolation regions.

6. (Original) The method of claim 1 wherein said device is fabricated on said substrate together with a plurality of other devices and wherein said corner diffusion regions

are formed during a sequence of processes for forming source/drain extensions in some of said plurality of other devices.

7. (Original) The method of claim 1, wherein said device is a PMOSFET device, wherein said source/drain extensions are formed using a PLDD implant process, and wherein said corner diffusion regions are formed using a NLDD implant process.

8. (Original) The method of claim 1, wherein said device is a NMOSFET device, wherein said source/drain extensions are formed using a NLDD implant process, and wherein said corner diffusion regions are formed using a PLDD implant process.

9.-22. (Cancelled)

23. (New) The method of claim 1 wherein said corner diffusion regions are formed such that an on/off ratio of said device is determined by an extent said corner diffusion regions overlap with said first source/drain extension region.

24. (New) The method of claim 1 wherein said corner diffusion regions are formed such that a leakage current of said device is determined by an extent said corner diffusion regions overlap with said source/drain extension region.

25. (New) The method of claim 1 wherein each of said corner diffusion regions occupies an edge portion of said active area adjacent one of said isolation regions and extends from a surface of said substrate to a depth in said substrate that is close to a depth of the source/drain extension region.

26. (New) The method of claim 1 wherein said corner diffusion region extends under said gate.

27. (New) The method of claim 1 wherein a concentration of said dopants of said second conductivity type in said corner diffusion regions is comparable to a concentration of said dopants of said first conductivity type in said source/drain extension region.

28. (New) The method of claim 1, further comprising:

third and fourth corner diffusion regions in said substrate, said third and fourth corner diffusion regions overlapping with a second source/drain extension region in areas of said substrate adjacent said first and second isolation regions: and

wherein said second source/drain extension region includes dopants of a first conductivity type and said third and fourth corner diffusion regions include dopants of a second conductivity type that is opposite to said first conductivity type.

29. (New) The method of claim 1 wherein the device further comprises a gate dielectric layer under said gate, and wherein said corner diffusion regions are formed to reduce hot-carrier effects on said gate dielectric film.

30. (New) The method of claim 1 wherein said first and second isolation regions have divots near said active area and said corner diffusion regions are formed to reduce leakage current in said device associated with said divots.

31. (New) The method of claim 1 wherein said first and second isolation regions have sidewalls bordering said active area and said corner diffusion regions are formed to reduce leakage current near said sidewalls.

32. (New) The method of claim 1 wherein said corner diffusion regions overlap with said drain diffusion region in areas adjacent said first and second isolation regions.

33. (New) A method for fabricating a device on a substrate, comprising:
forming isolation regions in said substrate, said isolation regions defining an active area of the device and bordering at least two opposite sides of said active area;
forming a gate over said substrate and extending between said two opposite sides of said active area;
forming a first diffusion region and a second diffusion region in said substrate on opposite sides of said gate and extending between said two opposite sides of said active area;
forming a third diffusion region in said substrate between said gate and said first diffusion region and extending between said two opposite sides of said active area; and
forming a fourth diffusion region in said substrate between said gate and said second diffusion region and extending between said two opposite sides of said active area, said fourth diffusion region including two edge portions adjacent respective ones of said

isolation regions and a middle portion between said two edge portions, wherein said two edge portions are doped with dopants of a first conductivity type and with dopants of a second conductivity type in comparable concentrations, said first conductivity type being opposite to said second conductivity type, and said middle portion is doped primarily with dopants of a first conductivity type.

34. (New) The method of claim 33 wherein said two edge portions and said middle portion of said fourth diffusion region extend from a surface of said substrate to a depth in said substrate.

35. (New) The method of claim 33 wherein size of each of said two edge portions relative to that of said middle portion of said fourth diffusion region determines an on/off ratio of said device.

36. (New) The method of claim 33 wherein size of each of said two edge portions relative to that of said middle portion determines a leakage current of said device.

37. (New) The method of claim 33 wherein the device further comprises a gate dielectric layer under said gate, and wherein said dopants of said second conductivity type in said two edge portions of said fourth diffusion region serve to reduce hot-carrier effects on said gate.

38. (New) The method of claim 33 wherein the device is among a plurality of transistors in an integrated circuit and said dopants of said conductivity type were introduced into said substrate by exposing portions of said substrate corresponding to said two edge portions of said fourth diffusion region to an implant process for forming source/drain extension regions in some of said plurality of transistors.

39. (New) A method for fabricating a device on a substrate, comprising:
forming isolation regions in said substrate, including a first isolation region bordering a first side of an active area of the device and a second isolation region bordering a second side of said active area opposite to said first side;
forming a gate over said substrate and extending between said first and second sides of said active area;

forming a first diffusion region and a second diffusion region on opposite sides of said gate and extending between said first and second sides of said active area;

forming a third diffusion and a fourth diffusion region between said gate and respective ones of said first diffusion region and said second diffusion region, said third diffusion region and said fourth diffusion region extending between said first and second sides of said active area and from a surface of said substrate to a first depth in said substrate; and

forming a fifth diffusion region overlapping with said fourth diffusion region in an area of said substrate adjacent said first isolation region and a sixth diffusion region overlapping with said fourth diffusion region in an area of said substrate adjacent said second isolation region, said fifth diffusion region and said sixth diffusion region extending from a surface of said substrate to a second depth in said substrate, said second depth being close to said first depth; and

wherein said fourth diffusion region is doped with dopants of a first conductivity type and each of said fifth diffusion region and said sixth diffusion region is doped with dopants of a second conductivity type opposite to said first conductivity type, and wherein concentration of dopants of said second conductivity type in said fifth and sixth diffusion regions is comparable with concentration of dopants of said first conductivity type in said fourth diffusion region.

40. (New) The device of claim 39, further comprising:

a seventh diffusion region and an eighth diffusion region overlapping with said third diffusion region in areas of said substrate adjacent said first and second isolation regions and extending from a surface of said substrate to said second depth in said substrate, wherein said third diffusion region is doped with dopants of said first conductivity type and each of said seventh diffusion region and said eighth diffusion region is doped with dopants of said second conductivity type opposite to said first conductivity type, and wherein concentration of dopants of said second conductivity type in said seventh and eighth diffusion regions is comparable with concentration of dopants of said first conductivity type in said third diffusion region.

41. (New) The device of claim 39 wherein said fifth diffusion region and said sixth diffusion region overlap with respective portions of said second diffusion region adjacent said first and second isolation regions.

42. (New) A method for forming a substrate, comprising:

forming a gate over said substrate and extending across a width of said device;

forming a first diffusion region and a second diffusion region on opposite sides of said gate and extending across said width of said device;

forming a third diffusion and a fourth diffusion region between said gate and respective ones of said first diffusion region and said second diffusion region, said third diffusion region and said fourth diffusion region extending across said width of said device and from a surface of said substrate to a first depth in said substrate; and

forming a fifth diffusion region overlapping with said fourth diffusion region and extending across said width of said device and from a surface of said substrate to a second depth in said substrate, said second depth being close to said first depth; and

wherein said fourth diffusion region and said fifth diffusion region are doped with dopants of opposite conductivity types in comparable concentrations.

43. (New) The method of claim 42, further comprising:
- a sixth diffusion region overlapping with said third diffusion region and extending across said width of said device and from a surface of said substrate to said second depth in said substrate, wherein said third diffusion region and sixth diffusion region are doped with dopants of opposite conductivity types in comparable concentrations.
44. (New) The method of claim 42 wherein said device is a narrow width device.
45. (New) The method of claim 42 wherein said fifth diffusion region is formed to reduce an inverse narrow width effect associated with said device.
46. (New) The method of claim 42 wherein said fourth diffusion region and said fifth diffusion region extend between two shallow trench isolation regions formed in said substrate that define said width of said device, and said fifth diffusion region is formed to reduce leakage current in said device associated with said shallow trench isolation regions.